Abstract

An input level translator circuit is provided. The translator circuit is configured to convert a full-range signal into a low-range signal and a high-range signal. A first pass transistor is configured to restrict the voltage of the full-range signal to provide a high-range voltage at a high-range node when the full-range signal corresponds to a logic 0. A second pass transistor is configured to restrict the voltage of the full-range signal to provide a low-range voltage at a low-range node when the full-range signal corresponds to a logic 1. A first switch circuit is configured to couple the high-range to a first cascode bias signal when the full-range voltage corresponds to a logic 1. A second switch circuit is configured to couple the low-range node to a second cascode bias signal when the full-range voltage corresponds to a logic 0.